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PAGE INDEX NOTES

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SUPPORTING INFORMATION

CATEGORY	NUMBER
None.	

COMMON SYSTEMS

3ACC MAINTENANCE PROGRAMMERS' MANUAL

AT&TCo Prov

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39 PAGES

BELL TELEPHONE LABORATORIES, INCORPORATED

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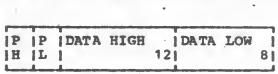
TABLE OF CONTENTS

1. MAINTENANCE CHANNEL

1.01 The maintenance channel (MCH) is used for communication between central controls (CCs), as well as diagnosis of one CC by the other. Each MCH can control the MCH in the other CC and exercise it at a very basic level. The basic structure of an MCH is shown in Fig. 1. It consists of a transmit receive register (MCHTR), a command register (MCHC), a buffer register (MCHB), and various gating paths to and from the CC. The MCH has the ability to decode the command part of the received message and perform various operations as a result.

1.02 The format of a MCH message is 22 bits of data and parity and 8 bits of command.

1.03 The data is in the same format as for the 20-bit gating bus, ie, 20-bits of data and 2 parity bits. For 16-bit data fields, the high 4 bits of the data-high field are not used. For 12-bit data fields, only the data-high field is used with its parity bit PH.



Maintenance Channel Commands

1.04 Table A shows the maintenance channel commands. BST (bit stream timing) indicates that timing is derived from the bit stream from the other CC. All other commands use clock timing from this CC.

TABLE A

MAINTENANCE CHANNEL COMMANDS

MNEMONIC	ACTION IN RECEIVING MCH	CONDITIONAL ON	4-OUT-OF-8[1] CODE (HEX)
CLER	Clear ER		65
CLMSR	Clear MSR		35
CLPT	Clear PT	CC=0	C5
CLTT0	Clear Timer Timeout Register		2D
DISA	Disable A		A5
DISB	Disable B		E1
INITCLK	Initialize Clock ((BST)[3]	CC=0	47
LDMAR	Clear STP;MAR← MCHTR;Set FRZ	CC=0	4D
LDMCHB	MCHB← MCHTR		99
LDMIRH	MIRH← MCHTR	STOP OR FRZ	8D
LDMIRL	MIRL← MCHTR;Execute One Cycle	STOP OR FRZ	1D
MSTART	Clear Freeze	CC=0	C9
MSTOP	Set STP	CC=0	D1
RTNER[2]	MCHTR← ER;Transmit (BST)		8B
RTNMB[2]	MCHTR← MB;Transmit (BST)		A3
RTNMCHB[2]	Transmit		B1
RTNMMH[2]	MCHTR← MMH;Transmit		55
RTNMML[2]	MCHTR← MML;Transmit		95
RTNSS[2]	MCHTR← SS;Transmit (BST)		93
SPCLK	Stop the Clock (BST)	CC=0	17
STCLK	Start the Clock (BST)		C3
SWITCH	Hardware Initialization (BST)	CC=0	0F
TOGCLK	Toggle Clock Input (BST)	CLK STOPPED	27

[1]Includes 3-out-of-7 command plus the start bit.

[2]These commands require a zero data-field format in the transmitted message.

[3]BST (bit stream timing).

CLER — Clears the other CC's error register (ER).

CLMSR — Clears the other CC's maintenance state register (MSR).

CLPT — Causes the other CC's program timer (PT) to be cleared. This command is performed independent of any normal CC control or data paths. If this is attempted in an on-line processor, the command is not executed and an error signal is generated.

CLTTO — Clears the timer timeout register (TTO) which clears the backup timing counter (BTC) after it has been set for a fixed period of time. In order to keep the other CC's program timer (PT) blocked, the TTO must be cleared periodically.

DISA — Causes the first disable signal to be sent to the other CC's I/O disable circuit.

DISB — Causes the second disable signal to be sent to the other CC's I/O disable circuit.

INITCLK — Initializes the clock to phase 3. The running or stopped status of the clock is not affected by this command.

LDMAR — Resets the STP flip-flop, loads the other CC's micro-address register (MAR) with the low 12 bits of the data field, and sets the FREEZE flip-flop, which freezes the MAR contents. The controlled CC must be stopped and off-line prior to this command's execution.

LDMCHB — Causes the 20-bit data field and 2 parity bits to be loaded into the other processor's maintenance channel buffer register (MCHB).

LDMIRH — Causes the data field to be gated to the other CC's MIR for one microcycle. This command is executed only if the other CC is stopped or frozen.

LDMIRL — Causes the data field to be gated to the microinstruction register (MIR) low 16 bits and the resultant TO and FROM control fields to be active for a single cycle. This command is executed only if the other CC is stopped or frozen.

MSTART — Resets the FREEZE flip-flop allowing the other CC to start processing microinstructions at the address frozen in the MAR. This command is performed only if the CC flip-flop is cleared (off-line).

MSTOP — Sets the STP flip-flop which jams the MAR to a maintenance address resulting in all zeros being read out of the microstore. This command is performed only if the CC flip-flop is cleared (off-line).

RTNER — Returns error register (ER) from the other CC. The ER is gated to the MCHTR and transmitted back, independent of any normal CC control or data paths.

RTNMB — Returns miscellaneous bits (MB) from the other CC. The MB is gated to the MCHTR and transmitted back independent of any normal CC control or data paths. See Table B.

TABLE B

MISCELLANEOUS BITS

MB BIT	SYMBOL[1]	SOURCE
0	CLKP0	P01 - Clock Phase 0
1	CLKP1	P11 - Clock Phase 1
2	CLKP2	P21 - Clock Phase 2
3	CLKP3	P31 - Clock Phase 3
4	MANKEY	Manual Key
5	SDSAB	Semi-Disable FF
6	SENAB	Semi-Enable FF
7	DISAB	Disable FF
8	PWRKEY	Power Key
9	TMRSW	Test Mode Reversal Switch
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		

[1]These symbols are defined in a Common Systems library.

RTNMCHB Causes the contents of the MCHB in the other processor's maintenance channel to be gated to its MCHTR and transmitted back.

RTNMMH Causes the high 16 bits of the microstore word currently addressed by the microaddress register to be gated to the MCHTR and transmitted back.

RTNMML Causes the low 16 bits of the microstore word currently address to the microaddress register to be gated to the MCHTR and transmitted back.

RTNSS Returns the system status register (SS) from the other CC. The SS is gated to the MCHTR and transmitted back independent of any normal CC control or data paths.

SPCLK Stops the clock with phase 3 active. This command may only be performed in the off-line CC.

STCLK Starts the clock with the phase 3 to phase 0 transition.

SWITCH Performs a hardware initialization of the other CC in order to switch it on-line. This command is performed only if the CC flip-flop is cleared (off-line). If the CC flip-flop is set (on-line), an interrupt is generated to the on-line CC.

TOGCLK Causes the other CC's clock to be advanced half a phase. This command is used when the other CC's clock has been stopped to manually step it through all its states. This command may only be performed in the CC.

Example of MCH Usage

1.05 The following steps are necessary in order to send a message over the MCH to the other CC.

(a) Load the MCHTR with the appropriate data. Use the load special register command (LSR) for 16-bit fields and PACK for 12- or 20-bit fields.

(b) The LMCH macro, which has the MCH command as an operand, generates the instructions which load the MCHC and branch to a subroutine which starts the MCH transmitting. It takes about 8 USEC, excluding the overhead of setting up the MCH and checking for completion, for the MCH to complete its transmission and receive the response from the other CC during which time the MCH goes through the following steps.

1. Start transmission.

2. After the message is transmitted, the MCH continues sending timing pulses and looks for a received message.

3. After the received message has been received into the MCHB, the MCH enters the idle state.

(c) The MCH transmit subroutine checks for the completion of the MCH function by timing beyond the maximum time necessary and then checking the complete and error flip-flops by gating them to the C register and testing them. The CF will be set for a normal completion and cleared for an abnormal completion of the MCH.

(d) Gate the MCHB contents to their destination using LRS or UNPK. For many MCH commands, there is no meaningful return data and this step will not be performed. The other CC's MCH will always respond with the return code in the command field, and in those cases where no meaningful data is returned, the data transmitted will be returned.

MCH Program

1.06 The following 3A CC program reads the high 16 bits of the other CC's microstore at an arbitrary address.

```
LMCH    MSTOP           #STOP THE OTHER CC
BNCL    MCHERROR        #TEST ERROR FLAG
LAL     2,ADDRESS,12
LR      2,12
LR      3,13
PACK    MCHTR           #LOAD MICROADDRESS IN MCHTR
LMCH    LDMAR           #PUT ADDRESS IN OTHER
                        #CC'S MAR
BNCL    MCHERROR        #TEST ERROR FLAG
LMCH    RTNMMH          #GET THE HIGH 16 BITS OF
                        #MICROMEMORY FROM THE
                        #OTHER CC
BNCL    MCHERROR        #TEST ERROR FLAG
```

THE MICROMEMORY CONTENTS ARE NOW IN THE ONLINE MCHB.

2. CONTROL BITS

2.01 The 3A CC control bits are grouped into three status registers: SS, MCS, and MMSR. Many of the control bits in the status registers have special paths into their inputs or out of their outputs as indicated in the following descriptions.

TABLE C

SYSTEM STATUS REGISTER

BIT	SYMBOL[1]	FUNCTION	DIRECT SET[2]	DIRECT CLEAR[2]
0	AME	Address Match Enable		
1	BHC	Block Hardware Checks	M	
2	BIN	Block Interrupts		
3	BTC	Block Timers	M	D
4	DME	Data Match Enable		
5	HLT	Halt Mode		
6	ISC1	Initialization Sanity Check 1		P
7	ISC2	Initialization Sanity Check 2		P
8	LOF	Lock Off-Line	X	X
9	LON	Lock On-Line	X	X
10	MAN	Manual Mode	X	
11	MINT	Microinterpret Mode		M,D
12	CC	On-Line, Off-Line Mode		P
13	REJ	CC Panel Reject Bit		
14	STP	Stop Mode	X,D	M
15	DISIO	Disable I/O Mode	DISABLE FF	
16	PRI	Priviledge Instruction Mode		
17	DISP	Display Bit		
18	BPC	Block Gating Bus Parity Check		
19	IPLTRK	IPL Track Bit		
PL	CC0	CC Identification Bit		
PH	CC1	CC Identification Bit		

---

[1]These symbols are defined in a Common Systems library.

[2]X=External signal
M=Hardware initialization
D=Decoder cross-point
P=Power on signal.

System Status Register (SS)

2.02 Table C shows the bits of the system status register (SS).

2.03 Address Match Enable (AME) - The AME bit enables the match between the store address register and the address input register.

2.04 Block Hardware Checks (BHC) - The BHC bit disables the output of the error register which switches processors.

2.05 Block Interrupt (BIN) - The BIN bit disables all interrupts.

2.06 Block Timer Check (BTC) - The BTC bit blocks the input and output from the program timer.

2.07 Data Match Enable (DME) - The DME bit enables the match between the store data register and the data input register.

2.08 Halt (HLT) - The HLT bit drives the panel lamp which indicates that the CC is in a program-halt condition ie, not executing main memory instructions. The HLT bit is set during every loop of the off-line microprogram and cleared by the hardware initialization sequence as well as the off-line microprogram before it services an interrupt.

2.09 Initialization Sanity Check 1 (ISC1) The ISC1 bit is used to check the sanity of the hardware initialization routine. The use of the ISC1 bit is shown in Fig. 2. The failure detected by this bit will result in a switch to the other central control.

2.10 Initialization Sanity Check 2 (ISC2) - The ISC2 bit is used to check the sanity of the hardware initialization routine. The use of the ISC2 bit is described in 6.06. The failure detected by this bit will result in the reloading of memory.

2.11 Lock Off-Line (LOF) - The LOF bit disables the I/O channels so that the locked off-line CC cannot interfere with the system. The LOF bit is set by a signal from the system status panel.

2.12 Lock On-Line (LON) - The LON bit forces all hardware switch messages to initialize this CC in order to keep it on-line. The LON bit is set by a signal from the system status panel.

2.13 Manual (MAN) - The MAN bit, monitored by software, drives the manual lamp on the CC panel. The manual key on the 3A CC control panel physically controls this bit and must be active to enable the reset circuits key and execute key functions.

2.14 Microinterpret Mode (MINT) - The MINT bit blocks the gating from the micromemory into the microinstruction register (MIR) and enables the gating from the main memory into the MIR. The MINT bit is reset by a miscellaneous decoder crosspoint.

2.15 Central Control (CC) - The CC bit indicates whether the CC is on-line (CC=1) or off-line (CC=0) and controls various functions, most of which protect the on-line CC from interference by the off-line CC.

2.16 Reject (REJ) - The REJ bit drives the CC panel lamp which indicates that a panel operation has been rejected by the CC.

2.17 Stop (STP) - The STP bit jams the micro address register (MAR) to a maintenance address causing all zeros to be read out of micromemory. The STP Bit can be set by hardware check circuits or by a CC or maintenance channel crosspoint (the latter two only if the CC is off-line). The STP bit can be cleared by a hardware initialization signal or a maintenance channel crosspoint.

2.18 Disable I/O Mode (DISIO) - This bit when set indicates that the 3A CC I/O main channels are disabled.

2.19 Priviledge Instruction Mode (PRI) - This bit serves as a microcode status bit for the auxiliary processor instruction set.

2.20 Display (DISP) - The DISP bit enables the gating from the PA to the DB on all transfers when it is set.

2.21 Block Bus Parity Check (BPC) - The BPC bit disables the program gating bus parity check.

2.22 Initiate Program Reload Track Bit (IPLTRK) - When set it causes the IPL microprogram sequence to read track 2 of the tape cartridge.

2.23 Central Control 0 (CC0) - The CC0 bit is always 1 in CC0 so that the program can determine the CC in which it is running.

2.24 Central Control 1 (CC1) - The CC1 bit is always 1 in CC1 so that the program can determine which the CC in which it is running.

Micro Control Status Register (MCS)

2.25 The microprogram control status register (MCS) can be directly gated to the bus but cannot be gated into from the bus. Table D shows the bits of the MCS.

TABLE D

MICRO CONTROL STATUS REGISTER

BIT	SYMBOL[1]	COPY
0	CF	0
1	CF	1
2	DS	0
3	DS	1
4	TR1	0
5	TR1	1
6	TR2	0
7	TR2	1
8	DR	0
9	DR	1
10	RU	0
11	RU	1
12	IFF	0
13	IFF	1
14	OPF	0
15	OPF	1
16	MARP	0
17	MARP	1
18	ERU	0
19	ERU[2]	
PL	PL	01
PH	PH	01

[1]These symbols are defined on all Common Systems library as the concatenation of symbol and copy.

[2]This is a buffered output of the same flip-flop that controls bit 18 above.

2.26 Condition Flip-Flop (CF) - The CF bit is used as a branch condition for the microprocessor. The CF bit is set and reset by miscellaneous decoder (MD) crosspoints and also may be gated to from other control bits.

2.27 Data Manipulation Logic Status (DS) - The DS bit is used as a branch condition for the microprocessor. The DS bit is set and reset according to the results of certain data manipulation logic operations and also may be gated to and from an I/O channel to indicate its status.

2.28 Test Register 1 (TR1) - The TR1 bit is used as a branch condition for the microprocessor. The TR1 bit is set and reset by MD crosspoints and also may be gated to from an I/O channel to indicate its status.

2.29 Test Register 2(TR2) - The TR2 bit is used as a branch condition for the microprocessor. The TR2 bit is set and reset by MD crosspoints and also may be gated to from an I/O channel to indicate its status.

2.30 Data Ready (DR) - The DR bit is used to indicate that the last main memory operation has been completed. The DR bit is set by a combination of the store completion signals from both stores and reset by any signal which initiates a main memory operation.

2.31 RAR Update (RU) - The RU bit controls the function of the RAR. When RU equals 1, the RAR is used as a duplicate of the microaddress register to check the gating into it from the microinstruction register and the micromemory. When RU equals 0 the RAR is used to save a return address which will subsequently be branched to, eg, return from a subroutine. The RU is set by the same control signal that gates out of the RAR and reset by MD crosspoint.

2.32 I Flip-Flop (I) - In applications where main memory words exceed 16 bits, a second SDR and SIR are required (see Fig. 2). The I bit determines from which SIR the new op-code is derived (SIR0 for the low 16 bits of memory and SIR1 for the upper bits of memory field).

2.33 Opcode FIL (OPF) - The OPF bit is used when expanding the number of operation codes from 128 to 256. If the OPF bit equals 0, the 7-bit op field maps into a block of 128 opcodes starting at microstore address 256. If the OPF bit equals 1, the opcode field maps into a block of an additional 128 opcodes starting at microstore address 2048.

2.34 MARP - The MARP bit is an internal check function as opposed to the control functions performed by other bits in this register. In general, it reflects the parity of the MAR.

2.35 Error Return Address Update (ERU) - The ERU bit controls the function of the Error Return Address Register (ERAR). When the ERU=1, the ERAR is continually updated from the microstore next address (NA) field. Under the conditions that the system is not in the double store read (DSR) mode, that a Store Error C (SERC) signal is returned from the store, and that microcontrol is testing for main memory completion, the hardware:

(a) Clears the ERU flip-flop, which inhibits updating the ERAR

(b) Jams 0777 (octal) into the MAR and executes the complement correction subroutine.

At the end of the complement correction subroutine, a miscellaneous decoder crosspoint sets the ERU and gates the ERAR to the MAR.

Main Memory Status Register (MMS)

2.36 The MMS controls the processor bus controller (PBC) which is the CC's interface to and from the main memory. The MMS can be gated to the GB and thereby to any destination of the GB. When gating to registers with fewer than 18 bits, an UNPK command must be used. The MMS may only be gated into from the low 16 bits of the B register by use of an MD crosspoint. Table E shows the bits of the MMS.

TABLE E

MAIN MEMORY STATUS REGISTER

BIT	SYMBOL[1]	COPY
0	MM1	0
1	MM1	1
2	MM2	0
3	MM2	1
4	RW	0
5	RW	1
6	IDLE	0
7	IDLE	1
8	UPD	0
9	UPD	1
10	ISO	0
11	ISO	1
12	BDSR[2]	0
13	BDSR	1
14	CW	0
15	BEC[2]	0
16	CW[3]	
17	BEC[3]	

2.37 Memory Maintenance 1(MM1) and Memory Maintenance 2(MM2): The MM1, MM2, and RW bits are decoded into eight possible states of the store command leads (SC3 through SC0) as defined in Table F.

2.38 Read or Write (RW): The RW bit determines whether the memory is being requested to perform a read or a write.

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[1] These symbols are defined on a Common Systems library as the concatention of symbol and copy.

[2] See Table G

[3] These are buffered outputs from the same flip-flops as bits 14 and 15, respectively.

TABLE F

STORE COMMAND STATES

RW	MM2	MM1	SC3	SC2	SC1	SC0	DESCRIPTION
1	0	0	1	1	0	0	Normal Read
1	1	0	1	0	1	0	Spare
1	0	1	1	0	0	1	Maintenance Read
1	1	1	1	1	0	0	Normal Read with Lock[1]
0	0	0	0	0	1	1	Normal Write
0	1	0	0	1	0	1	Spare
0	0	1	0	1	1	0	Maintenance Write
0	1	1	0	0	1	1	Normal Write with Lock[1]

2.39 IDLE: The IDLE bit, if it is set, disables all communications to its corresponding memory. One of the IDLE bits (copy 0) controls this store and the other bit controls the other store; consequently, they should always be the complement of each other.

2.40 Update (UPD): The UPD bit determines whether or not the off-line memory is to be updated. If it is set, all writes are sent to the off-line memory as well as to the on-line memory, regardless of the IDLE bit status.

2.41 Isolate (ISO): The ISO bit prevents the other CC from accessing this CC's memory.

2.42 Complement Write (CW): The complement write bit when set will cause the contents of the last word read from the MAS to be complemented and then written into memory at the same location from which it was read.

---

[1]Lock forces the store request (SRQ) signal to remain active as long as lock is active in order to retain control of the store bus.

TABLE G

SYSTEM RESPONSES ON MAIN STORE READS

MACRO CALL	AC OPTION	SYSTEM USE	STATE BDR	STATE BEC	STATE OMAS[1]	NUMBER OF PARITY ERRORS 0	1	2
L_ONL(X)	DSR	Normally duplex mode (double store read)	0	0	1	A	D[2]	D[2]
LOS(X)	DSR	None	0	0	1	A	A[2]	A[2]
L_ONL(X)	NO	Diagnostic MAS read	0	1	0	A	A[2]	A[2]
LOS(X)	NO	Diagnostic other MAS read	0	1	1	A	A[2]	A[2]
L_ONL(X)	COM	Normal simplex mode (complement correction)	1	0	0	A	B[2]	C
LOS(X)	COM	None	1	0	1	A	A[2]	C
L_ONL(X)	YES	MAS audit	1	1	0	A	A[2]	C
LOS(X)	YES	MAS audit, normal other Mas read	1	1	1	A	A[2]	C

Key:

A Return actual data (including bad parity, if any) as is.

B Cause microinterrupt to do complement correction and then return complemented data, ie, original data.

C Return complemented data, ie, original data for a previously complement corrected location.

D Access the other MAS and return the actual data.

L_ONL - Load Online Store Data into R0
LOS - Load Other Store Data into R0
AC Option - Automatic Correction Option

---

[1] OMAS=0 means CC is accessing its own MAS.
OMAS=1 means CC is accessing the other MAS.

[2] SERC signal generated.

Status Bits Stored In Memory

2.43 Out of Service (OS): The OS bit indicates that an abnormal condition that will prevent the CC from being put on-line as the result of a normal switch, is present.

2.44 Store Out of Sync (SOS): The SOS bit indicates that the on-line and off-line stores are not in sync.

3. INTERRUPTS

3.01 The interrupt facility, as shown in Fig. 3 allows interrupts at 16 different levels in the IS register. Each of these levels can be individually masked by the 16 bits of the IM register. All unmasked bits of the IS register are ORed together and used to jam set the MAR to a fixed location if the BIN flip-flop is not set. The BIN flip-flop, when set, blocks all interrupts. The microcontrol, when jammed to the fixed location, searches for the highest priority interrupt and services it.

3.02 Table H shows the assignment of bits in the IS, with bit 0 being the highest priority and the priority decreasing as the bit position increases. The bits in the interrupt mask (IM) register are assigned correspondingly since each bit masks the corresponding bit in the IS.

TABLE H

INTERRUPT SET REGISTER (IS)

BIT	SYMBOL[1]	FUNCTION
0		
1	UTILI	Utility Interrupt (External)
2		
3	ADMI	Address or Data Match
4		
5	ERRI	Error Register (INT CLass)
6		
7	OCCI	Other CC (External)
8		
9	TCI	Hardware Interrupt (Timing Counter)
10	TTYEI	TTY and Tape - Even (External)
11	TTYOI	TTY and Tape - Odd (External)
12		
13	MANI	Manual Panel Execute
14		
15		

4. ERROR REGISTER

4.01 Error signals are divided into four types: those that result in a switch to the other CC, those that cause a hardware initialization, those that cause an interrupt, and bit 10 that indicates a store read parity error (see Table I). The error signals that result in a switch are in error register (ER) bits 0 through 9, the ones that result in a hardware initialization are in ER bits 11 through 13, and the ones that result in an interrupt are in ER bits 14 through PH. The ER and its associated output circuits are shown in Fig. 4.

4.02 The signals from bits 0 through 9 are ORed together and the resulting signal is gated with the block hardware check bit. The resulting signal is ORed with the switch message from the program timer; this signal is normally (LON=0) used to stop the CC and send a switch message to the other CC. When the CC is locked on-line (LON=1), it is initialized instead of switched.

[1]These symbols are defined in a Common Systems library.

4.03 The signals from bits 11 through 13 are ORed together, gated with the block hardware check bit, and sent to the hardware initialization circuit.

4.04 The signals from bits 14 through PH are ORed together and then sent directly to the interrupt set register. This interrupt level can be blocked by setting the corresponding interrupt mask bit.

4.05 Bit 10 indicates a store read parity error has occurred.

TABLE I

ERROR REGISTER

BIT	SYMBOL[1]	FUNCTION
0	TODER	To Decoder Error
1	FRMDER	From Decoder Error
2	IBER	IB X,Y Field Error
3	BUSER	Gating Bus Parity Error
4	DMLER	DML Match
5	MARER	MAR Parity Error
6	CLKER	Clock Error
7	MSTRER	My Store Error (Error A)
8	MADER	MAR-RAR Match
9	FRER	Function Register Parity
10	SRPE	Store Read Parity Error (Error C for MY Store and Other Store)
11	MSTWRP	MY-Store Write Protect (Error B)
12	MFSTM	MY-Store Fast Timeout
13	BAFR	Branch Allowed Error
14	OWRTER	Other-Store Write Protect
15	OSTRER	Other-Store Error
16	OFSTM	Other-Store Fast Timeout
17	IOMLTER	I/O Multiple Channel Select
18	PTRER	PT Reset Received by On-Line CC
19	SWER	Switch Redeived by On-Line CC
PL	IOER	I/O Channel Error
PH	IOPARER	I/O Bad Parity Received

5. I/O ENABLE CIRCUIT

5.01 Normally, it should not be necessary to disable the off-line CC since, by definition, the off-line CC should not interfere with the on-line CC. However, in order to handle the case of a fault in the off-line CC that would cause it to interfere with the on-line CC, it is necessary to provide a facility for disabling the off-line CC. It is necessary to provide the on-line CC with the ability to disable the off-line CC; however, this means that the off-line CC could also potentially disable the on-line CC! Each CC must also be able to enable itself, if the PT signals an initialization, and restart in order to prevent the situation where both CC's are disabled. However this provides the potential for the bad off-line CC to enable itself! In order to protect the system from the occurrence of either of these problems, it is proposed that the enable function have several states. Fig. 5 shows the state diagram of the enable circuit. In this diagram, state 0 is the normal enabled state, and state 2 is the normal disabled state. States 1 and 3 are transition states which should only exist for a short period of time during normal operation. Their function is to prevent faults from erroneously changing the enable circuit's output. In order to better understand how the enable circuit operates, following is a description of normal circuit operation.

5.02 Suppose that CC0 desires to disable CC1. The sequence of actions which CC0 must perform are shown in Fig. 6. CC0 must first send a DISA message to CC1 via the MCH which will put the CC1 enable circuit in state 1. Next, CC0 must run detection tests whose successful completion ensures that CC0 is running properly. CC0 finally sends a DISB message to CC1 which puts the CC1 enable circuit in state 2 and disables CC1. This sequence of events ensures that a faulty CC will not be able to disable the other CC.

5.03 Next, suppose that CC0 has been disabled, but the problem that caused the disabling has been corrected, and it is desired to have CC0 enabled again. First, CC0 activates its control signal ENA by means of the appropriate microinstruction. This takes the CC0 enable circuit to state 3 from the normal disable state 2. Next, CC0 runs a series of detection tests whose successful completion ensures that CC0 is functioning properly. Finally, CC0 activates its control signal ENB which takes the enable circuit from state 3 to state 0, the normal enable state. Because of this sequence of events, a faulty CC will not be able to enable itself and interfere with the good CC.

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[1]These symbols are defined in a Common Systems library.

5.04 The enable circuit is used to enable the I/O channels as shown in Fig. 7. Although a bad CC could interfere with a good CC's memory by operating in double-store mode, the good CC can protect itself by setting its ISOLATE bit. The combination of the enable circuit and the ISOLATE bit allow the good CC to always protect itself from interference by a bad CC.

6. HARDWARE INITIALIZATION

6.01 A hardware initialization (HI) may be performed any time that a signal is received from one of the following sources:

(a) Program timer (PT), first or second timeout
(b) System status panel initialization signal
(c) Error register
(d) Switch request via the MCH
(e) Power turn on
(f) Reset circuits switch on CC panel.

6.02 When the power turnon switch is turned on, the following sequence of functions is performed which result in placing the CC in a stable off-line state:

(a) A portion of the CC power is turned on. This portion inhibits outputs from the I/O.

(b) The I/O and remaining CC power is turned on.

(c) A power initialization signal does the following:

(1) CC=0
(2) PT partially cleared
(3) I/O channels disabled
(4) ISC1=0
(5) ISC2=0
(6) Hardware initialization (via reset circuits key).

6.03 When power is turned off (this can only be done if the lock off-line (LOF) bit in the system status (SS) register is one), the I/O channel power is turned off, followed by the CC power.

6.04 The HI proceeds in three stages: first, some things are initialized by hardware before the first microcycle; second, a microprogram does some more initialization; and third, a main store program does more initialization and determines the source of the initialization in order to decide what action is to be taken following the initialization.

6.05 The following items are initialized by hardware before the first microcycle of the HI sequence:

(a) BHC=1
(b) STP=0
(c) MINT=0
(d) MSR=0
(e) CLOCK=P3
(f) FRZ=0
(g) MAR=X OBF
(h) BTC=1
(i) Initialize MCH.

6.06 The hardware initialization microprogram follows.

(a) Initialize RAR.

(b) Save SS --> AI.

(c) Clear MRFMCH INHIBIT FF and decoder maintenance status.

(d) Initialize the first 10(0-9) I/O main channels.

(e) Initialize the IB and the function register.

(f) Zero SDR1.

(g) Save: PA --> AK, IS --> DI, IM --> DK.

(h) Set interrupt mask to allow panel and other CC interrupts only.

(i) Zero the opcode FIL and I bits.

(j) Zero SS register bits AME, DME, HLT, DISP, REJ, and SP2.

(k) Clear the IS.

(l) Set the main memory status register equal to 3CB0.

(m) If the RESET CKT FF equals 1, zero the BIN FF, zero the CC FF, and go to the HALT loop. If the RESET CKT FF equals 0, go to (n).

(n) Enable I/O and then send a main store initialization message twice.

(o) If the ISC1 equal to 0, set ISC1 equal to 1 and begin the main memory initialization program at location 20 hex (40 octal). If the ISC1 equals 1, idle the maintenance channel switch sequencer and proceed to (p).

(p) If ISC2 equals 0, set ISC2 equal to 1, set ISC1 equal to 0 and stop and switch to other CC. If ISC2 equals 1, SS --> BR and reload main memory from tape (IPL SEQ).

6.07 When the microprogram transfers to main memory it executes the program shown in Fig. 8; the basic function of this program is to determine whether the CC is to be on-line or off-line after the HI is complete.

7. MICRO INTERPRET

7.01 The microinterpret instruction (MI) puts the CC in interpret mode in which main memory words are interpreted as microinstructions, ie, the 16 bits from main memory are used as the two 8-bit TO and FROM control fields.

Description of the Microinterpret Instructions

7.02 The MI instruction allows an arbitrary number of microinstructions to be executed following it. The MI instruction places the CC in microinterpret mode by setting the MINT bit. Each following main memory word is interpreted as a microinstruction until the microinstruction which clears the MINT bit is given, after which the CC returns to normal. Only a linear string of microinstructions may be performed with the MI instruction since the microinstructions are fetched from main memory in sequential fashion, without the address portion. Every time a branch is desired, the interpret mode must be cleared and a main instruction branch done. Since the address portion of the microinstruction is not used in interpret mode, a data fetch from micromemory can not be done either and data must be fetched from main memory using main memory instructions. Interrupts are not serviced while the CC is in interpret mode.

Implementation

7.03 The microprogram which implements the MI instruction, sets the MINT bit, fetches the next main memory word, and transfers to the all-zeros address where it waits for the data ready (DR) bit to indicate that the next word is ready. When the DR bit becomes a one, the contents of the store instruction register (SIR) are gated to the MIR and the low-order bit of the MAR is set to one. The CC executes the control fields in the MIR and then goes to address 1 which initiates a main memory fetch and goes to location X. At location X, a branch is done to the all-zeros address.

Programming

7.04 The MIMODE macro which can generate either an MI or MIS instruction should always be used.

8. MAINTENANCE STATE REGISTER

8.01 The maintenance state register (MSR) sets up conditions in the CC for testing purposes. The MSR should be cleared during normal processing since most of the conditions set up by the MSR will cause errors. Three of the clock test leads are decoded at the clock, but all the other MSR bits are independent. The functions of the MSR bits are shown in Table J.

Clock Test Conditions

8.02 The three clock test bits MSR(1,2,3) are decoded into the following states shown in Table K.

TABLE K

CLOCK TEST BITS

MSR(1,2,3)	NAME	FUNCTION
000	CNOP	Normal or no-operation
001	P0AL	Force P0A low
010	P0AH	Force P0A high
011	P1AH	Force P1A high
100		Spare
101	P0BL	Force P0B low
110	P2BH	Force P2B high
111	P3BH	Force P3B high

TABLE J

MAINTENANCE STATE REGISTER

BIT	SYMBOL[1]	FUNCTION
0	OVLOF	Override LOF
1	CLK1	Clock Test Conditions
2	CLK2	Decoded As
3	CLK3	Described Below
4	STRGO	Ground MY-STORE Go Lead
5	BUSBY	Ground Bus Busy Lead
6	FREEZ	Utility Freeze
7	MCMPT	Ground MY-STORE Complete Lead and MY-STORE Busy Lead and Inhibits OTHER-STORE Complete. Also Force Error C.
8	OCMPT	Ground OTHER-STORE Complete Lead and OTHER-STORE Busy Lead and Inhibit MY-STORE Complete
9	XYGATE	Enable IB(X,Y) to MIR When Stopped and Partially Inhibit from Check
10	MCADCMP	Enable RAR-MAR Match Independent of RU Flip-Flop Plus Diverts Store GO Flip-Flops Into Store Write Protect Error Bits
11	DISMARP	Hold MAR Parity
12	DIST0	Disable TO-FIELD Decoder
13	COM1	Code Merger Test 1 Also Enable ERAR to MAR Gating Path
14	COM2	Code Merger Test 2
15	STRIS	Jam Store Control Lead 3 = 1
PL		Allows MCH to be Active to Execute LMMIRL or LDMIRH
PH		Reenables MAR Parity Checker When the Stop Flip-Flop is Sent and Sends a Maintenance State to the Main Store to Enable Other 3A CC'S I/O Port

[1]These symbols are defined in a Common Systems library.

9. SYSTEM STATUS PANEL

9.01 The system status panel (SSP) is used to display the status of major system blocks and also provide a system interface for situations requiring direct manual interaction. The SSP is partitioned into two functional groups, the system status and control (SSC), which reflects the general system condition, and the system emergency manual control (SEMC) which is used to stabilize a system via manual intervention during an emergency situation, eg, repeated system timeouts. Communication between the SSP and CCs is via coax cable as shown in Fig. 9. The data transmitted over the coax cable are in the form of bipolar pulses which can be interpreted as either ones or zeros at the CCs.

I/O Format

9.02 The SSP circuits require the following 21-bit I/O message format:

BIT POSITION	20	19 ... 12	11	10 ... 5	4	3	2 ... 0
CONTENT	PH	DATA	PL	3/6 ADDRESS	OP CDE		START CODE

9.03 The start code is always 011 while the opcode may be either a 01 for a write-read operation (writes data into flip-flop memory specified by address field and immediately read and transmit back to CC for comparison) or a 10 for a read-only operation. Reception of a message with a non-normal start code or bad parity results in the immediate transmission to both CCs of the message just received with a maintenance start code (101) and an all-zeros data field.

9.04 The SSC portion of the SSP is primarily a display of system health. Generally the display reflects the state of a flip-flop memory element in the SSP controller circuit which is in most cases controlled, and in all cases readable, via I/O messages from the CCs. The only lamps or key/lamps not associated with a flip-flop logic element are circuit power, lamp test, and lamp power.

9.05 The SEMC has several functions that require interaction of various keys and circuit logic. In general, all logic function keys are non-locking push-push action (push to set, release, and then push to reset, etc). The notable exception to the push-push keys are the following nonlocking keys (NL): alt bus (ALT), alarm release, and lamp and power test. Also the following keys are mechanically locking: disable remote access, circuit power, and lamp as appear on board power.

9.06 In the following list of key operations for SEMC and SSC, an NW preceding each description means the program cannot set or clear the related panel function logic (but may still interrogate bit status).

System Initialization

9.07 The following sequence is required for each initialization attempt.

(a) (NW) ENABLE: Operate enable key (observe enable lamp bit)

(b) Stable Calls, Recent Change/Past Office Data, Memory Reload: Select and operate appropriate initialization key (any combination or none of these if basic level initialization is desired) and observe key lamp is lit.

(c) EXECUTE: Operate EXECute key. This action will extinguish the enable lamp via hardware and generate a single MRF pulse to both CCs. The CC program will initiate I/O messages that will interrogate the initialization level and then reset the initialization level and execute flip-flops.

9.08 To abort the procedure in 9.07 (prior to execution), manually reset all keys.

TTY INIT

9.09 The TTY key sets a flip-flop which is interrogated by the program and acted upon accordingly.

EMER LINE TRFR (NW)

9.10 The EMER LINE TRFR key sets the corresponding flip-flop which operates a relay that provides contact closure to appropriate central office equipment. This causes selected phone service to be switched to an alternate phone system when this system can no longer process calls. This state can be manually activate only!

DISABLE REMOTE ACCESS

9.11 This mechanical locking key when in the off state holds the related flip-flop cleared. The program continually attempts to set this flip-flop but is only able to do so when the key is operated. The output of the flip-flop is only used to light the related lamp as the key contacts actually perform the disabling function.

NOTE: Remote switching control centers (SCC) may still read the key and lamp status when the key is operated, although the SCC can no longer control SSP switch functions.

FORCE ACTIVE

9.12 Either CC may be forced active (set appropriate LON or LOF bit in system status register) by use of the select CU/SYC 0 or select CU/SYC 1 keys and the force key. First either the select CU/SYC 0 or select CU/SYC 1 key must be operated (these functions are mutually exclusive via hardware circuit interlocks) and then the force key is operated. Under these conditions a steady stream of pulses[1] is sent to each CC, forcing the selected CU/SYC active and the other CU/SYC to the unavailable state. If the previously active CU/SYC was selected, the system is merely locked to the existing state. If a CU/SYC switch occurs, a program-initiated basic level initialization occurs. Higher levels of initialization may be achieved while the forcing function is active by following procedures outlined herein under system initialization. To retire the force function, any force active key may be operated, but to retire the selected CU lamp, that key itself must be operated.

LOCK (NW)

9.13 The LOCK key automatically provides the same hardware function as the force active switches when forcing the active CU/SYC active and the other CU/SYC unavailable. The appropriate force active keys will light as if manually operated. Subsequent operation of any of these keys will tear down the lock function (although if a force active key is operated, the same restrictions apply as stated under part 5). Two separate flip-flops are associated with the LOCK key.

LOCKM Manually set or cleared by manual operation of key.

LOCKP Set by program message only if LOCKM is set. LOCKP remains set after LOCKM is manually cleared to allow the program to clear the force active circuits. The LOCKP is cleared via software control.

TEST CONTROL

9.14 The test control section provides visual indication (PASS or FAIL) of a test sequence previously set up via TTY messages and initiated via the PF EXECUTE key.

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[1] A positive lobe of a bipolar pulse is sent to the selected active 3A CC and a negative lobe is sent to the nonselected 3A CC.

ALARM CONTROL

9.15 Each key listed under alarm control is application oriented, but basically sets a flip-flop which is interrogated by the CU program. In the case of INH BLDG ALM and ALARM XFER, provides a relay interface to central office circuits is provided. Alarm release is set via software only but may be cleared by manually operating the key.

MAJOR EQUIPMENT LOST

9.16 This lamp acts as a beacon for an application controlled group of peripheral alarms.

10. TEST MODE SWITCH

10.01 The test mode switch is provided in order to be able to use the 3A CC panel functions in an on-line machine.

10.02 The functions of the test mode switch are to override the blocking of the execute switch by the CC flip-flop and to override the blocking of the reset circuits switch by the CC flip-flop.

10.03 The switch is accessed by gating it to the DB as part of one of the switch registers. Access is necessary in order for the microprogram to decide whether to halt or interrupt when compare interrupt is received.

11. I/O CHANNEL AND SUBCHANNEL ASSIGNMENT

11.01 The assignment of main channel 0, subchannels 2, 3, and 7 is coded in the microprogram. The remaining subchannels are available for Common System and application usage as required. Table L defines a possible assignment of subchannels in I/O channel 0 (code 000111).

TABLE L

NO. 3 ESS CHANNEL 0 SUBCHANNEL ASSIGNMENTS

SUBCHANNEL	CODE	ASSIGNMENT
0	0001111	System Status Panel
1	0010111	Spare
2	0011101	Tape 0
3	0011110	Tape 1
4	0100111	Spare
5	0101101	TTY
6	0101110	TTY
7	0110011	MY Memory
8	0110101	OTHER Memory
9	0111001	Spare
10	1000111	Fast Distributor
11	1001011	Network
12	1001101	Network
13	1010011	Slow Distributor
14	1010101	Slow Distributor
15	1011001	Slow Distributor
16	1100011	Scanner
17	1100101	Scanner
18	1101001	Scanner
19	1110001	Scanner

11.02 Subchannels 0 through 9 are on subchannel board 1 and subchannels 10 through 19 are on subhchannel board 2.

12. SWITCH REGISTERS LAYOUT

12.01 There are three sets of panel switches or switch registers which can be gated to the DB. The assignment of bits in these registers to panel switches is shown in Table M.

TABLE M

SWITCH REGISTER 1

	SWITCH NAME		
BIT	SWITCH REG 1	SWITCH REG 2	SWITCH REG 3
0	Enable Manual Parity	Register Select 1	Input Key 0
1	Step Mode	Register Select 2	Input Key 1
2	Halt Mode	Register Select 4	Input Key 2
3	Basic Mode	Register Select 8	Input Key 3
4	Display Register	Special-General Reg	Input Key 4
5	Load Register		Input Key 5
6	Reset Circuit		Input Key 6
7	Test Mode		Input Key 7
8	Compare Data		Input Key 8
9	Compare Address	Power Key	Input Key 9
10	Manual		Input Key 10
11			Input Key 11
12	Memory - Display		Input Key 12
13	Memory - Store		Input Key 13
14	Memory - Increment Address		Input Key 14
15	Memory - High Bits		Input Key 15
16			Input Key 16
17			Input Key 17
18			Input Key 18
19			Input Key 19
PL			Input Key PL
PH			Input Key PH

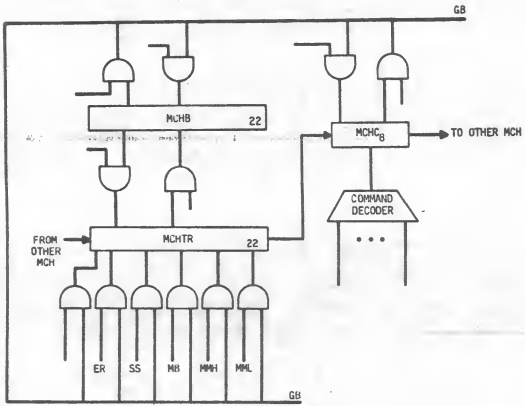


Fig. 1 - Maintenance Channel Functional Diagram

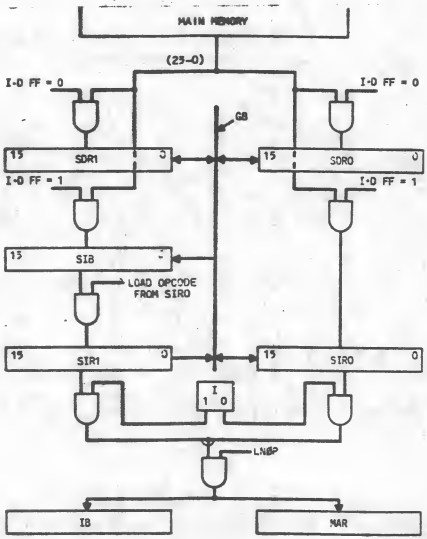


Fig. 2 - No. 3A CC with 2B Main Memory Interface

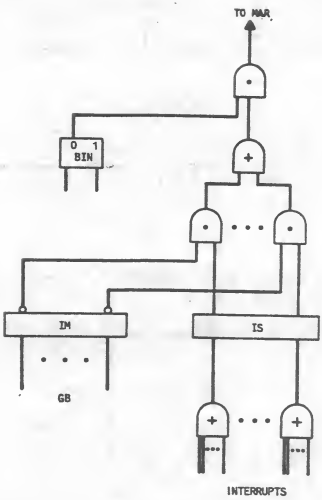


Fig. 3 - Interrupt Logic

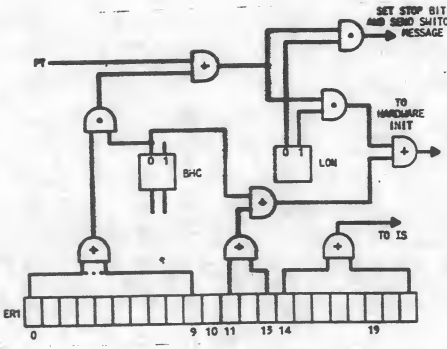
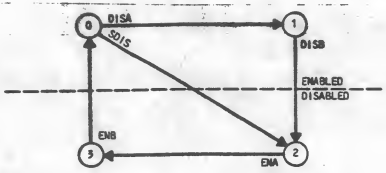


Fig. 4 - Error Registers



INPUT NAME	FROM	MEANING
ENA	CONTROL	FIRST ENABLE
ENB	SIGNAL	SECOND ENABLE
SDIS	DECODER	SELF DISABLE
DISA	MAINTENANCE	FIRST DISABLE
DISB	CHANNEL	SECOND DISABLE

Fig. 5 - Enable Circuit

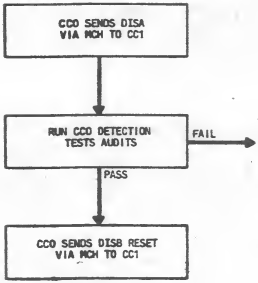


Fig. 6 - CC0 Disabling CC1

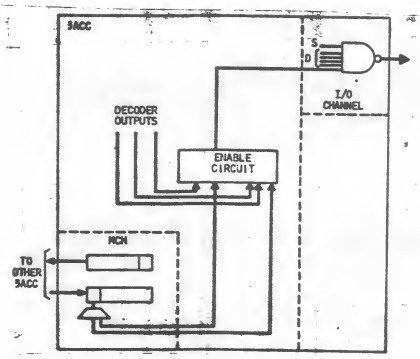


Fig. 7 - Enable Control

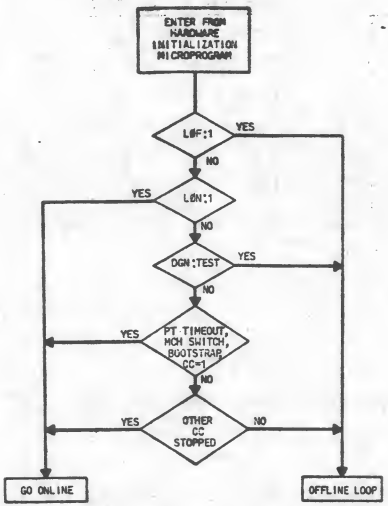


Fig. 8 - Hardware Initialization Main Program

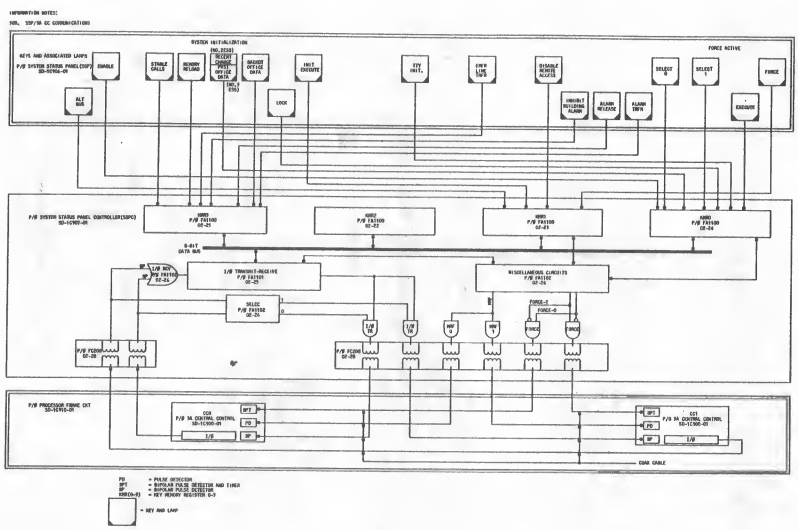


Fig. 9 - System Status Panel/3A CC Communication